Detailed Syllabus

Semester: I

Course Title: Digital Logic **Full Marks: 60+20+20**
Course no: BIT 103 **Pass Marks: 24+8+8**
Nature of course: Theory + Lab **Credit hours: 3**

Course Description:

This course familiarizes students with Number System, Digital Design Fundamentals, Understand and Design Functions of Combinational Logic, Sequential Logic (Counters, Registers and Finite State Machine), Memories, Programmable Logic Devices Integrated Circuit Technologies.

Course Objective:

To provide the concepts used in the design and analysis of digital systems and introduces the principles of digital computer organization and design.

Course Contents:

Unit 1: Number Systems, Operations and Codes (6 Hrs.)	**Teaching Methodology**	**Teaching Hours**
History of Number System, Introduction to Number System (Positional and Non positional), Decimal, Binary, Octal, Hexadecimal Number Systems	Lecture	1
Conversion from one number system to another (Binary, Octal, Hex to Decimal; Decimal to Binary, Octal and Hex; Binary to Octal, Octal to Binary, Binary to Hex, Hex to binary)		2
Compliment of Number Systems (r's complement and r-1's compliment with r as 2 and 10)		1
Addition and Subtraction of Binary Numbers, Binary Codes (Absolute, Gray Code, weighted binary code, BCD, ASCII, Unicode) and Error Detection Codes		2
Unit 2: Digital Design Fundamentals and Boolean algebra (8 Hrs.)		
Digital and Analog Signals (Definition, example and difference between them)	Lecture/Lab	1
Logic Operations (Definition and Truth Table of AND, OR, NOT)		1
Introduction to the System Concept, Logic Gates (Basic Gates, Derived Gates, Universal Gates)		2
Logic Function and Boolean Algebra (*characteristics, laws, simplifications using laws, principle of duality*)		4
Unit 3: Simplification of Boolean Functions (5 Hrs.)		
K-map, Two and Three variable maps, Four variable maps, product of sum simplification	Lecture	2
NAND and NOR implementation, Don't Care conditions		2

Unit 4: Combinational Logic (7 Hrs.)		
Adders and Subtractors (Half and full binary adder and subtractor), Parallel Binary Adders		2
Multiplexers and Demultiplexers		2
Encoders and Decoders, Seven segment decoder		2
Code Converters, Magnitude comparator (2 bit and 4 bit)		1
U**nit 5: Sequential Logic (4 Hrs.)**		
Latches and Flip-Flops (*RS, JK, D, T, Master-Slave*), Edge-Triggered Flip-Flops	Lecture/ Lab	2
Flip-Flop Operating Characteristics, Flip-Flop Applications		2
Unit 6: Counters, Registers and Memory (9 Hrs.)		
Asynchronous Counters, Synchronous Counters, Up/Down Counters, Counter Applications	Lecture/ Lab	3
Basic Shift Register Operations, Shift Register Types, Bidirectional Shift Registers, Shift Register Counters		3
Basic Memory Operations and memory types (*ROM, PLA, PAL*)		3
Unit 7: Processor Logic Design (6 Hrs.)		
Processor Organization, Arithmetic Logic Unit, Design of Arithmetic Circuit, Design of Logic Circuit, Design of Arithmetic Logic Unit (*one bit ALU design only*) Status Register, Design of Shifter (*4 bit combinational logic shifter*)	Lecture/ Lab	6

Text Book:

- Mano M.M., *Digital logic and Computer Design*, Pearson Education

References Books:

- Mano M.M. and Ciletti M. M, *Digital Design*, 4thedition
- Brown S. and Vranesic Z., *Fundamentals of Digital Logic with VHDL Design*, 3rd edition, McGraw Hill
- Rafiquzzaman M., *Fundamentals of Digital Logic and Microcomputer Design*, 5th edition, JohnWiley & Sons, Inc.
- Holdsworth B. and Woods C., *Digital Logic Design*, 4th edition
- Mano M. M, Kime C. R , *Logic and computer design fundamentals*, 2nd edition

Laboratory work in Digital Logic

The following lab activities are carried out using Digital Logic Kit, Bread board and Simulator.

1. Familiarization with Logic Gates
2. DeMorgan's law and its familiarization with NAND and NOR gates
3. Encoder, Decoder, Multiplexer and Demultiplexer, Seven segment display
4. Familiarization with Binary Addition and Subtraction
5. To realize a. Half Adder and Full Adder and Half Subtractor and Full Subtractor by using Basic gates and NAND gates
6. Implementation of true complement generator
7. Implementation of RS and T type flip flops
8. Implementation of D and JK type flip flops
9. Ripple Counter, Synchronous counter
10. Conversion of parallel data into serial format
11. Generation of timing signal for sequential system
12. Familiarization with PLAs and PLDs

Model Question

Level: BIT First Year/First Semester **Time: 3 Hrs** **F.M: 60**
Sub: Digital Logic (BIT 103) **P.M: 24**

Attempt <u>any two</u> questions. (2x10=20)

1. Design the full adder circuit using 3 to 8 decoder and explain the working principle.
2. What is JK master slave flip-flop? Design its logic circuit, truth table and explain the working principle.
3. The term LOGIC GATES is to be transmitted as 12 bytes of data. Each character in the term has an ASCII value. The system uses odd parity and left most bit is used as parity bit. An additional parity byte is also sent after the term. The following bytes have arrived at their destination.

		1	2	3	4	5	6	7	8
	letters	bytes received							
1	L	0	1	0	0	1	1	0	0
2	O	0	1	0	0	1	1	1	1
3	G	1	1	0	0	0	1	1	1
4	I	0	1	0	0	1	0	0	1
5	C	0	1	0	0	0	0	1	1
6	<space>	0	0	1	1	0	0	1	0
7	G	1	1	0	0	0	1	1	1
8	A	1	1	0	0	0	1	0	1
9	T	0	1	0	1	1	0	0	0
10	E	0	1	0	0	0	1	0	1
11	S	0	1	0	1	0	1	1	1
12	Parity byte	0	1	0	0	1	1	1	1

   a. One of the bytes has an error after transmission. Locate which character contains an error.
   b. Locate the bit that has been transmitted incorrectly.
   c. Explain how you have arrived at your conclusion.

Attempt <u>any eight</u> questions. (8x5=40)

4 Show that the dual of the exclusive-OR is equal to its complement.

5 Explain with state diagram and excitation table for 3-bit binary counter.

6 Design a decoder with three input lines but with only six output lines. If the value of the input corresponds to 6 or 7, then all output line should be asserted to signal an error.

7 What are the special characteristics of IC digital logic family? Explain them in brief.

8 A logic circuit implements the following Boolean function.

F=A'C+AC'D

It is found that the required input combination A=C=1 can never occur. Using K-map and proper don't care condition find simpler expression for F and implement it using not gate only.

9 a) Obtain the 9's and 10's complement of i) 13579 ii) 90090 decimal number.

b) Convert $(6524275)_8 = (?)_{16}$

10 Design 8 to 1 Multiplexer using two 4to 1 Multiplexers.

11 Given is a logic (switching) function F1 in the decimal list sum-of-minterms representation

$$\mathbf{F_1(A,B,C,D) = \Sigma(0, 2, 3, 5, 7)}$$

$$\mathbf{d(A,B,C,D) = \Sigma(8, 10, 13, 15)}$$

12 Write short notes on:

a. PLA

b. Triggering of flip-flop.